WHAT IS CLAIMED IS:

1. A tracing method, comprising:

obtaining at least one indication of a tracing condition, wherein a tracing condition defines a tracing control based upon a characteristic of an operating state of a processor;

detecting a change in said characteristic of said operating state of said processor; and effecting a predefined tracing control based on said detected change in said characteristic of said operating state of said processor.

- 2. The method of claim 1, wherein an indication is obtained via an input control signal.
- 3. The method of claim 1, wherein an indication is obtained via a software-settable trace control register.
 - 4. The method of claim 1, wherein said characteristic is a processor mode.
- 5. The method of claim 4, wherein said processor mode is one of a kernel mode, a supervisor mode, a user mode, and a debug mode.
- 6. The method of claim 5, wherein said kernel mode, said supervisor mode, said user mode, and said debug mode are based on the MIPS32 and MIPS64 architecture specifications.

- 7. The method of claim 1, wherein said characteristic is an identity of a process being run on said processor.
 - 8. The method of claim 1, wherein said effecting comprises initiating tracing.
 - 9. The method of claim 1, wherein said effecting comprises inhibiting tracing.
- 10. The method of claim 1, wherein tracing is triggered based on G, ASID, U, K, S, DM, and X controls, said controls enabling tracing when:
- (G is asserted OR (ASID equals a current process application space identity value))

 AND
 - (U is asserted AND said processor is in user mode) AND
 - (K is asserted AND said processor is in kernel mode) AND
 - (S is asserted AND said processor is in supervisor mode) AND
 - (DM is asserted AND said processor is in debug mode) AND
- (X is asserted AND (an exception level bit is asserted OR an error level bit is asserted).
 - 11. A tracing system, comprising:
 - a processor core for executing instructions; and

trace generation logic that detects a change in a characteristic of an operating state of said processor core, said trace generation logic effecting a predefined tracing control based on said detected change in said characteristic of said operating state of said processor.

- 12. The tracing system of claim 11, wherein said predefined tracing control is identified via an input control signal.
- 13. The tracing system of claim 11, wherein said predefined tracing control is identified via a software-settable control register.
- 14. The tracing system of claim 11, wherein said characteristic is a processor mode.
- 15. The tracing system of claim 14, wherein said processor mode is one of a kernel mode, a supervisor mode, a user mode, and a debug mode.
- 16. The tracing system of claim 15, wherein said kernel mode, said supervisor mode, said user mode, and said debug mode are based on the MIPS32 and MIPS64 architecture specifications.
- 17. The tracing system of claim 11, wherein said characteristic is an identity of a process being run on said processor.

- 18. The tracing system of claim 11, wherein said trace generation logic initiates tracing based on said detected change in said characteristic of said operating state of said processor.
- 19. The tracing system of claim 11, wherein said trace generation logic inhibits tracing based on said detected change in said characteristic of said operating state of said processor.
- 20. The tracing system of claim 11, wherein said trace generation logic triggers tracing based on G, ASID, U, K, S, DM, and X controls, said controls enabling tracing when:
- (G is asserted OR (ASID equals a current process application space identity value))
 AND
 - (U is asserted AND said processor is in user mode) AND
 - (K is asserted AND said processor is in kernel mode) AND
 - (S is asserted AND said processor is in supervisor mode) AND
 - (DM is asserted AND said processor is in debug mode) AND
- (X is asserted AND (an exception level bit is asserted OR an error level bit is asserted).
 - 21. A computer program product comprising:

computer-readable program code for causing a computer to describe a processor core for executing instructions; and

computer-readable program code for causing a computer to describe a trace generation logic that detects a change in a characteristic of an operating state of said processor core, said trace generation logic effecting a predefined tracing control based on said detected change in said characteristic of said operating state of said processor; and

a computer-usable medium configured to store the computer-readable program codes.

22. A method for enabling a computer to generate a tracing system, comprising: transmitting computer-readable program code to a computer, said computer-readable program code including:

computer-readable program code for causing a computer to describe a processor core for executing instructions; and

computer-readable program code for causing a computer to describe a trace generation logic that detects a change in a characteristic of an operating state of said processor core, said trace generation logic effecting a predefined tracing control based on said detected change in said characteristic of said operating state of said processor.

- 23. The method of claim 22, wherein computer-readable program code is transmitted to said computer over the Internet.
 - 24. A computer data signal embodied in a transmission medium comprising:

computer-readable program code for causing a computer to describe a processor core for executing instructions; and

computer-readable program code for causing a computer to describe a trace generation logic that detects a change in a characteristic of an operating state of said processor core, said trace generation logic effecting a predefined tracing control based on said detected change in said characteristic of said operating state of said processor.